

**BAE SYSTEMS**

**Mission Electronics Division  
PO Box 868, Nashua, NH 03060**

## **Bright Peak**

**Contract Value: \$550,467**

**Contract N00421-02-C-3029  
CDRL A002**

### **Contract Summary Report**

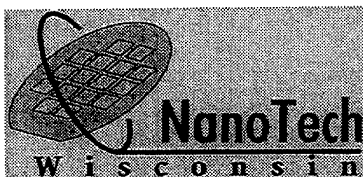
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**February 27, 2003  
Distribution Approved for Public Release; Distribution is Unlimited**

**20030310 119**



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**FINAL TECHNICAL REPORT ON YEAR ONE  
SUBCONTRACT FOR  
“Development of a Bright Peak Enhanced X-ray Phase  
Shifting Mask BPEXPM”**

**Under BAE Systems Contract entitled  
“MMIC T-Gate Fabrication Utilizing Phase-Shift Mask  
Technology with Single-exposure, Multi-layer X-ray Resist”**

Defense Advanced Research Projects Agency (DARPA) Contract N00421-02-C-3029 to BAE Systems and Subcontract RS9577 (UW 144-KY20) to the Center for NanoTechnology. This report covers the period 03/01/02 to 02/28/03 and the SOW were in response to BAA01-08.

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On February 25, 2003

**University of Wisconsin-Madison  
Center for NanoTechnology (CNTech)**

**FINAL TECHNICAL REPORT ON YEAR ONE SUBCONTRACT FOR  
 "Development of a Bright Peak Enhanced X-ray Phase Shifting Mask BPEXPM"  
 Under BAE Systems Contract entitled "MMIC T-Gate Fabrication Utilizing  
 Phase-Shift Mask Technology with Single-exposure, Multi-layer X-ray Resist"  
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**Executive Summary and Statements of Work (SOW).**

Under a separate DARPA grant, the Center for NanoTechnology (CNTech) had developed and patented (Yang, Lei, Taylor, J. W., and Cerrina, F., "Enhanced Bright Peak Clear Phase Shifting Mask and Method of Use", U. S. Patent 6,428,939, August 6, 2002, application filed 03/22/01) the concept of using a clear phase X-ray mask called the Bright Peak Enhanced X-ray Phase Mask (BPEXPM) to produce reduced features on the wafer from larger features on the mask. The reductions ranged from 5-6 such that a 250 nm mask feature would produce a 50 nm wafer feature, and a 100 nm mask feature would produce a 20 nm wafer feature. BAE Systems wanted to utilize the BPEXPM approach to the production of MMIC T-gate devices, and initiated a three-year subcontract with CNTech with the first year initially funded. This report summarizes the Statements of Work for that first year and briefly highlights the accomplishments. Further details and the plans for the second and third years are outlined in subsequent sections.

**SOW 1.A. Evaluate possible phase shifter materials that can be processed by normal semiconductor processing and show pin-hole free patterns. Start to 6 months.**

The results of this effort are shown in Table I below where CNTech beamlines can operate at 0.45, 0.8, and at 0.9 nm. Three good choices as Si, Si<sub>3</sub>N<sub>4</sub>, and PMMA.

**Table I. Phase Shifter Materials for 180° Shift as a Function of Wavelength.**

<b>Material (in <math>\mu\text{m}</math>)</b>			<b><math>\lambda</math> in nm</b>		
	<b>0.45</b>	<b>0.8</b>	<b>0.9</b>	<b>1.0</b>	<b>1.2</b>
<b>Be</b>	<b>5.00</b>	<b>2.78</b>	<b>2.46</b>	<b>2.20</b>	<b>1.82</b>
<b>Al</b>	<b>3.08</b>	<b>3.33</b>	<b>1.94</b>	<b>1.67</b>	<b>1.33</b>
<b>Au</b>	<b>0.75</b>	<b>0.45</b>	<b>0.4</b>	<b>0.36</b>	<b>0.31</b>
<b>Cr</b>	<b>1.26</b>	<b>0.70</b>	<b>0.62</b>	<b>0.57</b>	<b>0.49</b>
<b>Ni</b>	<b>0.97</b>	<b>0.56</b>	<b>0.52</b>	<b>0.49</b>	<b>0.50</b>
<b>Si</b>	<b>3.51</b>	<b>2.34</b>	<b>2.01</b>	<b>1.78</b>	<b>1.45</b>
<b>Si<sub>3</sub>N<sub>4</sub></b>	<b>2.87</b>	<b>1.45</b>	<b>1.26</b>	<b>1.13</b>	<b>0.93</b>
<b>TiN</b>	<b>1.72</b>	<b>0.94</b>	<b>0.84</b>	<b>0.76</b>	<b>0.64</b>
<b>SiC</b>	<b>2.56</b>	<b>1.59</b>	<b>1.38</b>	<b>1.22</b>	<b>1.00</b>
<b>Al<sub>2</sub>O<sub>3</sub></b>	<b>2.06</b>	<b>1.53</b>	<b>1.14</b>	<b>1.01</b>	<b>0.83</b>
<b>PMMA<sup>1</sup></b>	<b>6.25</b>	<b>3.48</b>	<b>3.08</b>	<b>2.78</b>	<b>2.31</b>

<sup>1</sup> PMMA is MW and density dependent; value of 1.19 g/cm<sup>3</sup> used here for 450 K.

Extensive modeling has been done on pattern size, phase shifter thickness at 45, 90, 120, 180, and 270 degrees and at the mask-to-wafer gap. One such illustration is shown in Figure 1.

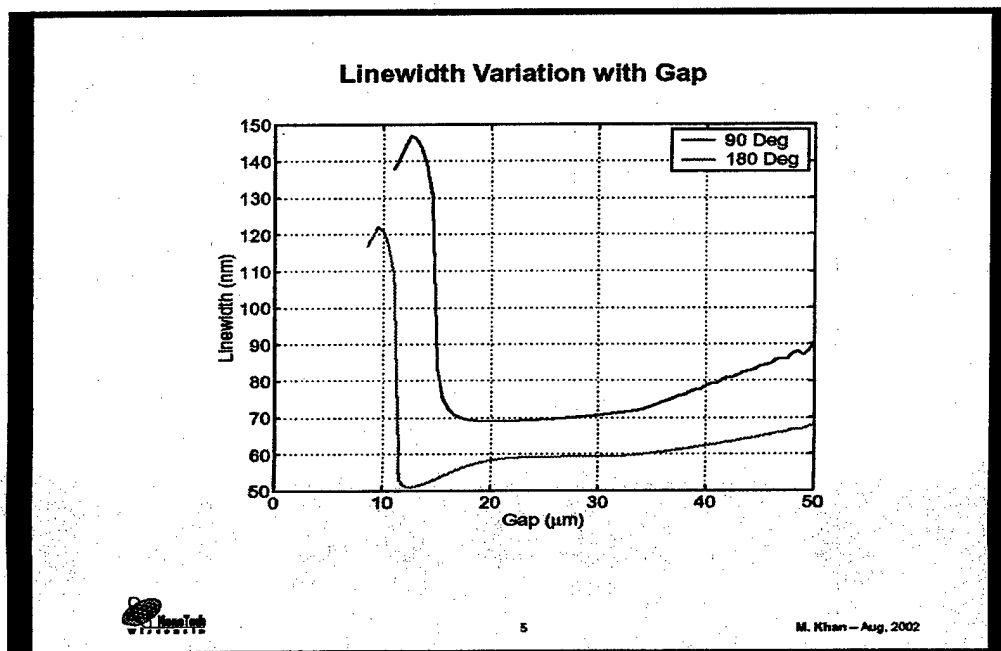


Figure 1. Silicon nitride phase mask modeling at 90 and 180° phase thickness for a 200 nm mask feature using 0.83 nm exposure radiation.

This figure shows that the 180° phase shifter would produce a 50 nm wafer feature, but the gap latitude is smaller than for a 90° thickness where the wafer feature is 70 nm. The optimum gap for the 50 nm feature is at 12 microns whereas the 70 nm feature is produced at a gap from 16 to 30 microns. This means that there is a gain in gap insensitivity but a loss in resolution by using a smaller thickness. Other studies show that thicknesses greater than 180° do not greatly improve the feature size reduction. This is shown in Table II.

Table II. Optimum Gap for a 200 nm PMMA Mask and LW for Resist Thresholds of 70% and 80% Using 0.9 nm Radiation.

Phase, deg.	Opt. Gap, $\mu\text{m}$	LW, nm <sup>1</sup>	LW, nm <sup>2</sup>
45	31.0	80.8	55.0
90	24.0	62.6	42.5
180	15.5	42.0	28.5
225	13.0	37.0	25.1
270	11.0	34.3	23.3

<sup>1</sup>LW measured at 70% of peak intensity.

<sup>2</sup>LW measured at 80% of peak intensity.

SOW 1. B. Evaluate the selected phase shifter materials for etch bias from e-beam written patterns that are from 400 to 150 nm in size. From six to 12 months.

What has been learned from modeling and from experiment is that the edge profile is a critical issue in the formation of these masks. If the edge varies much more than  $\pm 3^\circ$  from the vertical, the CD values become larger and do not show the same intensity enhancement. A similar observation was made for the single edge mask that prints into a negative-tone resist to make a trench. This aspect is illustrated in Table III.

**Table III. Modeling of Si<sub>3</sub>N<sub>4</sub> BPEXPM 200 nm Mask Feature at a Gap of 20  $\mu$ m.**

<u>Phase Shift, in <math>^\circ</math></u>	<u>Gap, <math>\mu</math>m</u>	<u>Slope</u>	<u>LW, nm at 70%</u>	<u>LW, nm at 85%</u>
90	20.0	- 4 $^\circ$	174.6	-
180	20.0	- 4 $^\circ$	170.8	151.6
90	20.0	0.0 $^\circ$	68.7	45.1
180	20.0	0.0 $^\circ$	56.6	37.1
90	20.0	+ 4 $^\circ$	56.4	38.1
180	20.0	+ 4 $^\circ$	50.8	34.6

This aspect of the development has proven to be a major obstacle in the device demonstration. CNTech has tried to get the edge profile by: utilizing an Al hard mask and using the etching facilities at Cornell; working with BAE Systems to develop a Ni lift off and Ni hard mask protection for the etching; using PMMA and solving the stress-crack issues; and etching of poly-silicon in the STS etchers in WCAM on campus. (The etchers on campus do not allow metal etching, so this was the reason that CNTech originally went to Cornell for the Al hard mask and teamed with BAE for the Ni hard mask.) Only the PMMA mask has demonstrated the BPEXPM in the dimensions required in the contract, but the mask feature arose from a fracture in the PMMA film rather than the patterned mask feature.

To date, the Ni lift off procedure has produced the correct edge for a silicon nitride phase shifter, and exposures are scheduled before the end of the 12 months of the subcontract. In addition, there has been substantial development in a process to create a stress-free PMMA mask. Exposures on this type of mask are in progress and will be completed before the end of the 12 month period. The etching of the poly-silicon has produced the necessary profile, but the etch also produce a scalloped edge structure that was deemed unsatisfactory for device exposures. Development work continues in solving the scalloping issue.

SOW 1.C. Design with BAE Systems a mask to be utilized to prove technology. From 10-12 months.

Several masks have been designed and written on the CNTech e-beam using the format of the DMS-217 Mask to create the edge phase mask structure associated with the negative resist program. The major finding from this study was that the alignment marks needed for the ALX alignment system on the Mod 4 stepper were easily read from the phase shift structures and that no metal alignment structures were needed. The writing of the BPEXPM masks for the device work has been done in PMMA for exposure at CNTech, and the exposure is in process at the current time.

We have also verified the correct position for the gap to obtain the maximum intensity and the line width using a 340 nm BPEXPM. In this case, the modeling predicted a minimum in the LW at a gap of 54 microns. Using Shipley XP-9947W at 115 mJ/cm<sup>2</sup>, the optimum gap was found to be 54 microns. These experimental results are a verification of the modeling for the BPEXPM, but this particular BPEXPM did not have the correct edge profile structure to produce the small CD that was predicted.

SOW 1. D. Utilize the technology to generate a 70 nm MMIC-gate structure utilizing the UW-Madison storage ring and the CNTech exposure stations. From 10-12 months.

CNTech has written BPEXPM structures on silicon nitride masks for etching by BAE, has written PMMA masks with the appropriate BPEXPM, and has worked with etching of a poly-silicon BPEXPM. We were expecting to expose a BPEXPM that might have the appropriate edge profile during the week of February 23<sup>rd</sup>, but one mask broke in the stepper, the PMMA mask showed cracks that indicated we had not determined the proper annealing and solvent development, and the poly silicon mask etching conditions still showed scalloping. The efforts are continuing on all three mask types, and we are confident that continuing efforts will produce the appropriate gate structure. The 70 nm gate structure should require a mask feature of 350 nm, and writing such a mask has not proven to be a problem at CNTech.

CNTech has explored the creation of mesa mask structures for the SiNH masks. The reason for this is that the optimum gaps for the BPEXPM exposures using a SiNH mask are on the order of 16 microns for a 90° phase shifter and 12 microns for a 180° phase shifter. To achieve these gaps in the Mod 4, the face of the mask needs to be flat to about 2 to 4 microns over the entire mask surface that faces the wafer to be printed. Directly creating a SiNH mask with these flatness specifications - 2 to 4 microns over the entire surface of the mask - is very difficult due to residual stresses in the mask. Holding to this specification would result in the rejection of many masks that otherwise might be useful if a process for improving the flatness could be devised.

In order to reach the gap for optimum printing of a particular BPEXPM, it is necessary that the combined non-flatness of the wafer, the wafer chuck, and the mask must be less than the gap necessary to do the printing. Tension in the nitride film produces bow in the mask blank that manifests itself as curl. This is most pronounced at the edges of the mask blank, whereas the center tends to be much flatter.

At CNTech this problem is addressed by the creation of a standard NIST mask that has material removed from the perimeter of the mask blank. This, in effect, creates a mesa mask so that the center of the mask, which contains the mask pattern and alignment targets, is retained. In the creation of the mesa structure, we have perfected a method for the removal of 50 to 100 microns of material from the outer portions of the mask blank where most of the non-flatness is

located. The resulting mesa masks allow us routinely to set gaps of 15 microns or less for the SiNH masks and do exposures at these gaps.

CNTech Approach to Forming a Mesa:  
(Exaggerated cartoon drawings. Not to scale.)

Nitride deposition. Some warp induced by tension in the nitride.



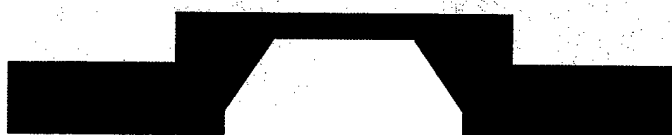
Backside etch of SiNH and Si to form freestanding membrane. Unbalanced tension in top surface nitride tends to form a concave surface.



Removal of nitride from front surface perimeter. Mask relaxes nearly flat.



Removal of 40 to 50 microns of Si from face makes certain that no contact will occur between mask and wafer during exposures.



SOW 1. E. Utilize the technology to generate 50 nm isolated lines from a bright peak mask using the UW-Madison storage ring and the CNTech exposure stations. From 10-12 months.

This effort is connected to the SOW above where we have written masks that have both types of mask structures to produce the appropriate wafer feature. In the case of the 50 nm line, a mask of 200 nm dimensions would be required. At nearly the end of the 12 months, however, we do not have exposures that demonstrate either the 70 nm gate structure or the 50 nm isolated line feature. Those results should come within the next two weeks, if the appropriate edge structure can be created in either the silicon nitride by Ni lift off, in the PMMA by appropriate choice of annealing and solvent development, or by improvements in the poly-silicon etching.

### Conclusions.

The potential application of the BPEXPM for device manufacture continues to be clearly possible once the mask edge issue can be solved. We have the resists with sufficient resolution to take the concept at least to the 50 nm level, but we currently lack a process to produce the necessary edge profile. The most promising approach is the utilization of poly-silicon because of its stability, but we are pursuing both the silicon nitride lift off with BAE and the PMMA masks to demonstrate feasibility. The application does clearly relax the need for high resolution masks and relaxes the narrow gap dependence that 1-X masks require. Further, the utilization of the BPEXPM for contact hole applications needs to be explored. As can be seen from Figure 1., it is possible to use a 90° phase shifter to provide a depth of focus of several microns. This is to be compared with current optical phase shift approaches where the dept of focus dependence is on the order of 0.15 microns.

It is also clear that one year of funding is not sufficient for the development of the BPEXPM to support device exposures. The critical finding of the importance of the edge profile created a problem that can be addressed with sufficient time and resources so that the BPEXPM can reach its full potential for device manufacture.